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Robin E. Barnum (Depositor's name)
[Signature] (Signature)
February 24, 2005 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,381	08/17/2001	Serge Lasserre	TI-31354	4434

TITLE OF INVENTION: LOCAL MEMORY WITH INDICATOR BITS TO SUPPORT CONCURRENT DMA AND CPU ACCESS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$1700	05/11/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
BRAGDON, REGINALD GLENWOOD	2188	710-022000

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1 Robert D. Marshall, Jr.2 W. James Brady, III3 Frederick J. Telecky, Jr.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

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Texas Instruments Incorporated

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

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Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

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☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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*Robert D. Marshall, Jr.*Date February 24, 2005

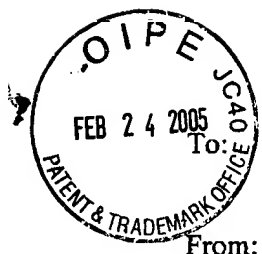
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

TI-31354

Serge Lasserre

Art Unit: 2188

Serial No.: 09/932,381

Examiner: Reginald G. Bragdon

Filed: August 17, 2001

Conf. No.: 4434

For: Local Memory With Indicator Bits to Support Concurrent DMA and CPU Access

CERTIFICATION OF FACSIMILE TRANSMISSION

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NAME OF INVENTOR(S): Serge Lasserre	
TITLE OF INVENTION: Local Memory With Indicator Bits to Support Concurrent DMA and CPU Access	
TI FILE NO.: TI-31354	DEPOSIT ACCT. NO.: 20-0668
FAXED: 2/24/05 DUE: 5/11/05 ATTY/SEC'Y: RDM/reb	
RECEIPT DATE & SERIAL NO.: Serial No.: 09/932,381 Filing Date: August 17, 2001	

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